* NOTICES *

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CLAIMS

[Claim(s)]
[Claim 1] It is the semiconductor device characterized by to be formed only in the perimeter the bottom of the field in which said wiring gutter is formed while opening for said etching stopper layer to form a connection hole in the semiconductor device equipped with the etching stopper layer formed between the layers of the insulator layer between the wiring layers in which a connection hole is formed, the insulator layer during wiring with which a wiring gutter is formed, and said two insulator layers is formed.
[Claim 2] Said wiring gutter is a semiconductor device according to claim 1 characterized by applying to said etching stopper layer and being formed from the insulator layer during said wiring.
[Claim 3] In the manufacture approach of the semiconductor device equipped with the process which forms the insulator layer between the wiring layers in which a connection hole is formed, the process which forms an etching stopper layer on the insulator layer between said wiring layers, and the process which forms the insulator layer during wiring with which a wiring gutter is formed The manufacture approach of the semiconductor device characterized by forming opening for forming a connection hole in said etching stopper layer while forming said etching stopper layer only in the perimeter the bottom of the field in which said wiring gutter is formed.
[Claim 4] The manufacture approach of the semiconductor device according to claim 3 characterized by applying to said etching stopper layer from the insulator layer during said wiring, and forming said wiring gutter in case said wiring gutter is formed in the insulator layer during said wiring.
[Claim 5] The insulator layer between said wiring layers is a semiconductor device which a wiring gutter is formed with the insulator layer between the wiring layers in which a connection hole is formed, and is characterized by forming the insulator layer between said wiring layers only in the perimeter the bottom of the field in which said wiring gutter is formed in the semiconductor device equipped with the insulator layer during wiring which has etch selectivity.

[Claim 6] The manufacture approach of the semiconductor device characterized by to form said connection hole in the insulator layer during said wiring while forming the insulator layer between said wiring layers only in the perimeter the bottom of the field in which said wiring gutter is formed in the manufacture approach of the semiconductor device equipped with the process which forms the insulator layer between the process which forms the insulator layer between the wiring layers in which a connection hole is formed, and wiring with which a wiring gutter is formed on the insulator layer between said wiring layers.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the semiconductor device which formed wiring structure by the dual DAMASHIN method, and its manufacture approach in detail about a semiconductor device and its manufacture approach.
[0002]
[Description of the Prior Art] Since copper wiring is put in practical use in recent years towards improvement in the speed of the working speed of a semiconductor device, and reduction of power consumption, development of a dual DAMASHIN process is performed. Moreover, a low dielectric constant insulating material is put in practical use and it is necessary to reduce wiring capacity. There are fluorine content silicate glass (FSG), organic film, a porous silica, etc. in a low dielectric constant ingredient.
[0003] It is important to control the wiring depth of flute by the dual DAMASHIN process correctly, in order to form wiring with sufficient homogeneity. therefore, the so-called first beer (FV) which forms a wiring gutter using good etching of the selectivity of the IMD film and the ILD film using an ingredient which is different by the insulator layer during wiring of the same wiring layer (IMD [say / the following and IMD film] is the abbreviation for Inter Metal Dielectrics), and the insulator layer between wiring layers (ILD [say / the following and ILD film] is the abbreviation for Inter Level Dielectrics) -- law is common. By this approach, since [being ****] it can kick, and there is nothing if it is **, the etch selectivity of the IMD film and the ILD film will be restricted to selection of an ingredient, and an ingredient with a high dielectric constant must be adopted as the ILD film. For example, an organic material is used for the IMD film and the silicon oxide system ingredient is used for the ILD film.
[0004] moreover, self-align [which arranges an etching stopper between the IMD film and the ILD film] dual DAMASHIN (SADD) -- law -- p.75-80 besides VMIC Conference Abstract and Y(1997).Morand It is indicated. The production process Fig. of drawing 7 explains the main processes of the SADD method below.
[0005] As shown in (1) of drawing 7 , the 1st insulator layer 111 of a wrap is formed for a component, wiring, etc. on the semi-conductor substrate (not shown) in which components, such as a transistor, and wiring were formed. The wiring 112 of the 1st of slot wiring structure is formed in this 1st insulator layer 111. The ILD film 121 is formed for the 1st wiring 112 by the wrap organic film on the 1st insulator layer 111 of the above. Furthermore, the etching stopper layer 122 is formed on the ILD film 121.
[0006] Then, as shown in (2) of drawing 7 , the opening 123 for carrying out opening of the connection hole to the etching stopper layer 122 is formed by the lithography technique and etching.
[0007] Next, as shown in (3) of drawing 7 , the wrap IMD film 124 is formed for opening 123 by the organic film on the above-mentioned etching stopper layer 122. Then, a hard surface mask blank 125 is formed by the oxidation silicate glass film on the IMD film 124.
[0008] Subsequently, as shown in (4) of drawing 7 , after forming the resist film 131 for forming a wiring gutter, the wiring gutter pattern 132 is formed in the above-mentioned resist film 131 with a lithography technique.
[0009] Then, as shown in (5) of drawing 7 , after using the above-mentioned resist film 131 for an etching mask, etching a hard surface mask blank 125 and the IMD film 124 and forming a wiring gutter 126, the etching stopper layer 122 is used for an etching mask, the ILD film 121 is etched, and the connection hole 127 is formed.
[0010] Subsequently, as shown in (6) of drawing 7 , after forming the barrier metal layer 128 in the above-mentioned

wiring gutter 126 and the connection hole 127, the barrier metal layer 128 is minded, and it is **********. Then, while removing the excessive copper on a hard surface mask blank 125, and a barrier metal layer (not shown) and forming wiring 129 through the barrier metal layer 128 in a wiring gutter 126 by chemical mechanical polishing (CMP [say / Following CMP] is the abbreviation for Chemical Mechanical Polishing), a plug 130 is formed through the barrier metal layer 128 in the connection hole 127.

[0011]

[Problem(s) to be Solved by the Invention] However, by the conventional FV method, in order to form in the whole surface the ILD film formed with an oxide film, even if it uses the low dielectric constant film for the IMD film, an effective dielectric constant cannot fully be reduced.

[0012] Moreover, by the SADD method, the etch selectivity of the IMD film and an etching stopper is needed. Therefore, the organic film is used for the IMD film and the ILD film, and the oxide film is used for the etching stopper. Thus, the oxide film which is an ingredient with a high dielectric constant must be adopted as an etching stopper. this SADD -- law -- FV -- if compared with law, an effective dielectric constant can be reduced, but in a Prior art, in order to form an etching stopper in the whole surface, even if it uses the low dielectric constant film for the IMD film and the ILD film, it has fully come to reduce an effective dielectric constant

[0013]

[Means for Solving the Problem] This inventions are the semiconductor device made in order to solve the above-mentioned technical problem, and its manufacture approach.

[0014] The 1st semiconductor device is the thing equipped with the etching stopper layer formed between the layers of the insulator layer between the wiring layers in which a connection hole is formed, the insulator layer during wiring with which a wiring gutter is formed, and these two insulator layers, and while the etching stopper layer is formed only in the perimeter the bottom of the field in which a wiring gutter is formed, opening for forming a connection hole is formed.

[0015] Since opening for forming a connection hole in the etching stopper layer is formed while the etching stopper layer is formed only in the perimeter in the 1st semiconductor device of the above-mentioned configuration the bottom of the field in which a wiring gutter is formed, there are few amounts of the etching stopper layer formed between two layers of an insulator layer as compared with the conventional etching stopper layer. Usually, since an etching stopper layer is with an ingredient with high dielectric constants, such as a silicon system oxide film and a nitride, and it is formed, by reducing the amount of an etching stopper layer in this way, the dielectric constant during wiring and between wiring layers is reduced, and the capacity between wiring and the capacity between wiring layers are reduced.

[0016] The process in which the manufacture approach of the 1st semiconductor device forms the insulator layer between the wiring layers in which a connection hole is formed, In the manufacture approach equipped with the process which forms an etching stopper layer on the insulator layer between wiring layers, and the process which forms the insulator layer during wiring with which covers an etching stopper layer and a wiring gutter is formed on the insulator layer between wiring layers While forming an etching stopper layer only in the perimeter the bottom of the field in which a wiring gutter is formed, it is characterized by forming opening for forming a connection hole in an etching stopper layer.

[0017] By the manufacture approach of the 1st semiconductor device of the above, since an etching stopper layer is formed only in the perimeter the bottom of the field in which a wiring gutter is formed, the amount of an etching stopper layer decreases as compared with the conventional etching stopper layer. Usually, although a dielectric constant will become high in order to form an etching stopper layer by the silicon system oxide film, a nitride, etc., the dielectric constant during wiring and between wiring layers is stopped by reducing the amount of an etching stopper layer in this way lower than the thing of the conventional configuration. Therefore, the capacity between wiring and the capacity between wiring are reduced.

[0018] Moreover, since opening for forming a connection hole is formed in an etching stopper layer while forming an etching stopper layer only in the perimeter the bottom of the field in which a wiring gutter is formed, it becomes possible to use an etching stopper layer as an etching mask at the time of forming a connection hole in the insulator layer between wiring layers. Furthermore, since the above-mentioned etching stopper layer is formed only in the perimeter the bottom of the field in which a wiring gutter is formed, when a wiring gutter is formed in the insulator layer during wiring, it will be formed on an etching stopper layer, without a wiring gutter protruding an etching stopper layer. Therefore, a wiring gutter is formed in the predetermined depth. Moreover, since an etching stopper layer is

formed also in the perimeter under the field in which a wiring gutter is formed even if a mask alignment gap occurs in the exposure process of a lithography process in case a wiring gutter is formed, an etching stopper layer is protruded and a wiring gutter is not formed. Therefore, what a wiring gutter is formed too much deeply and causes lower layer wiring and a short circuit does not happen.

[0019] A wiring gutter is formed with the insulator layer between the wiring layers in which, as for the 2nd semiconductor device, a connection hole is formed, and the insulator layer between wiring layers is formed only in the perimeter the bottom of the field in which a wiring gutter is formed in the thing equipped with the insulator layer during wiring with which the insulator layer between wiring layers has etch selectivity.

[0020] In the 2nd semiconductor device of the above-mentioned configuration, the volume of the insulator layer between wiring layers has become less than the insulator layer between the wiring layers currently formed with the conventional oxidation silicone film from being formed only in the perimeter the bottom of the field in which a wiring gutter is formed. Usually, when an oxidation silicone film lessens the insulator layer between the wiring layers which have such a high dielectric constant with about 4.2 dielectric constant since it is high, and are formed, the dielectric constant between wiring layers is reduced and the capacity between wiring layers is reduced.

[0021] The manufacture approach of the 2nd semiconductor device is characterized by to form a connection hole in the insulator layer during wiring in the manufacture approach equipped with the process which forms the insulator layer between the process which forms the insulator layer between the wiring layers in which a connection hole is formed, and wiring with which a wiring gutter is formed on the insulator layer between wiring layers while it forms the insulator layer between wiring layers only in the perimeter the bottom of the field in which a wiring gutter is formed.

[0022] By the manufacture approach of the 2nd semiconductor device of the above, since the insulator layer between wiring layers is formed only in the perimeter the bottom of the field in which a wiring gutter is formed, as compared with the former, the amount of the insulator layer between the wiring layers currently formed with the ingredient which has high dielectric constants, such as a silicon system oxide film, decreases. Thus, by reducing the insulator layer between wiring layers, the dielectric constant between wiring layers is stopped low. Therefore, the capacity between wiring is reduced.

[0023] Moreover, since the insulator layer between wiring layers is formed only in the perimeter the bottom of the field in which a wiring gutter is formed, when a wiring gutter is formed in the insulator layer during wiring, a wiring gutter separates from the insulator layer between wiring layers, and is not formed. Therefore, a wiring gutter is formed in the predetermined depth. Moreover, since the layer which has etch selectivity is formed also in the perimeter under the field in which a wiring gutter is formed even if a mask alignment gap occurs in the exposure process of a lithography process in case a wiring gutter is formed, an etching stopper layer is protruded and a wiring gutter is not formed. Therefore, what a wiring gutter is formed too much deeply and causes lower layer wiring and a short circuit does not happen.

[0024]

[Embodiment of the Invention] The outline configuration sectional view of drawing 1 explains the gestalt of the operation concerning the 1st semiconductor device of this invention. Drawing 1 shows an example of the semiconductor device formed by the approach of this invention based on the SADD method.

[0025] As shown in drawing 1 , the wrap insulator layer 11 is formed in a transistor, a capacitor, etc. which are formed on a semi-conductor substrate (not shown) like a silicon substrate (not shown). The wiring 12 of the 1st of slot wiring structure is formed in this insulator layer 11. Furthermore on the insulator layer 11, the ILD (Inter Level Dielectrics) film 13 used as the insulator layer between the wiring layers in which it is a wrap thing and a connection hole is formed in the 1st above-mentioned wiring 12 is formed at the thickness of 300nm. This ILD film 13 is formed for example, with the poly aryl ether. Or it may be formed by low dielectric constant organic film, such as BCB film, polyimide film, and amorphous carbon film.

[0026] Subsequently, on the above-mentioned ILD film 13, the etching stopper layer 14 is formed with the oxidation silicone film with a thickness of 150nm. While this etching stopper layer 14 is formed only on the bottom of the field which forms slot wiring, and the outskirts of it, the opening 15 for forming a connection hole is formed. With the circumference under the field which forms the above-mentioned wiring gutter, even if it causes a mask alignment gap in the exposure process at the time of forming a wiring gutter, it considers as the range where a wiring gutter is formed on the etching stopper layer 14. In addition, the above-mentioned etching stopper layer 14 may be formed with the acid silicon nitride film or the silicon nitride film.

[0027] On the above-mentioned ILD film 13, the IMD (Inter Metal Dielectrics) film 16 used as the insulator layer during wiring with which it is a wrap thing and a wiring gutter is formed in the above-mentioned etching stopper layer 14 is formed at the thickness of 300nm. This IMD film 16 may be formed by the insulator layer of the same ingredient as the above-mentioned ILD film 13, or may be formed by low dielectric constant organic film, such as BCB film, polyimide film, and amorphous carbon film.
[0028] On the above-mentioned IMD film 16, silicon oxide is deposited on the thickness of 200nm, it is formed, and the opening 18 which becomes the hard surface mask blank layer 17 with a wiring gutter pattern is formed for the hard surface mask blank layer 17. The connection hole 22 is formed in the ILD film 13 under the opening 15 which the wiring gutter 21 was furthermore formed in the ILD film 16 under the above-mentioned opening 18, and was formed in the above-mentioned etching stopper layer 14.
[0029] In addition, when a diffusion prevention layer like a silicon nitride film is formed on the 1st wiring 12, the connection hole 22 is formed so that a diffusion prevention layer may be penetrated and the front face of the 1st wiring 12 may be arrived at.
[0030] Furthermore the barrier metal layer 23 is formed in each inside of the above-mentioned wiring gutter 21 and the connection hole 22, the 2nd wiring 24 which consists of copper or a copper alloy is formed in the interior of a wiring gutter 21 through the barrier metal layer 23, and the plug 25 which consists of copper or a copper alloy is formed in the interior of the above-mentioned connection hole 22 through the above-mentioned barrier metal layer 23.
[0031] Furthermore, it is also possible to have formed the ILD film 13 same with above-mentioned having given explanation, the IMD film 16, the connection hole 22, a wiring gutter 21, the 2nd wiring 24, and plug 25 grade on the above-mentioned IMD film 16 and the 2nd wiring 24, and to have carried out the laminating of the above-mentioned wiring structure.
[0032] In the semiconductor device explained with the gestalt of implementation of the above 1st While the etching stopper layer 14 is formed only in the perimeter the bottom of the field in which a wiring gutter 21 is formed From the opening 15 for forming the connection hole 22 in the etching stopper layer 14 being formed SADD of the former [amount / of the etching stopper layer 14 formed between two layers with an insulator layer 13, i.e., the ILD film, and the IMD film 16] -- it has decreased as compared with the etching stopper layer formed of law. Usually, since the etching stopper layer 14 is formed using a silicon system oxide film, a nitride, etc. which are hard to be etched to the IMD film 16 of an organic material as explanation was given [above-mentioned], the dielectric constant is high. Like the gestalt of the above-mentioned implementation, by reducing the amount of the etching stopper layer 14, the effectual dielectric constant of the insulator layer currently formed between wiring (between the 2nd wiring 24 and 24) and between wiring layers (between the 1st wiring 12 and the 2nd wiring 24) is reduced, and the capacity between wiring and the capacity between wiring layers are reduced.
[0033] Next, the outline configuration sectional view of drawing 2 explains the modification in the gestalt of said explained operation. The same sign is given to the same thing as the component part shown by said drawing 1 in drawing 2 .
[0034] The configuration shown in drawing 2 is formed in the condition shown in said drawing 1 of a wiring gutter 21 penetrating the etching stopper layer 14, and reaching the ILD film 13 in the gestalt of the 1st operation, and the 2nd wiring 24 is formed in the interior of such a wiring gutter 21 through the barrier metal layer 23. Therefore, the lower part of a wiring gutter 21 is also formed in the etching stopper layer 14. The insulator layer 11 and the 1st wiring 12 which are other component parts, the ILD film 13, opening 15, the IMD film 16, the hard surface mask blank layer 17, opening 18, the connection hole 22, the barrier metal layer 23, the 2nd wiring 24, and plug 25 grade are the same as that of what was explained with the gestalt of said 1st operation.
[0035] With the configuration shown in above-mentioned drawing 2 , since the wiring gutter 21 was formed in the etching stopper layer 14, the volume has become less than the etching stopper layer 14 shown in drawing 1 . Therefore, the dielectric constant during wiring and between wiring layers only with the effectual part of the wiring gutter 21 formed in the etching stopper layer 14 is reduced.
[0036] Next, the production process Fig. of drawing 3 explains the gestalt of the operation concerning the manufacture approach of the 1st semiconductor device. In drawing 1 , an example of the semiconductor device formed by the approach of this invention based on the SADD method is shown, and the same sign is given to the same thing as the component part explained by said drawing 1 .
[0037] Although illustration is not carried out, after forming a transistor, a capacitor, etc. on a semi-conductor substrate

(for example, silicon substrate) (not shown), as shown in (1) of drawing 3 , an insulator layer 11 is formed. Subsequently, the 1st wiring 12 is formed in this insulator layer 11 with the slot wiring technique generally known, for example. The ILD (Inter Level Dielectrics) film 13 which is a wrap thing and turns into an insulator layer between wiring layers in the 1st wiring 12 on the insulator layer 11 is formed in the thickness of 300nm. After this ILD film 13 consisted for example, of the poly aryl ether and applied the precursor of the poly aryl ether by the rotation applying method, it was formed by 300 degrees C - 450 degrees C (here, as an example, it is 400 degrees C) heat treatment. In addition, it is also possible to use low dielectric constant organic film other than the poly aryl ether, such as for example, BCB film, polyimide film, and amorphous carbon film, for the ILD film 13.

[0038] Subsequently, the etching stopper layer 14 is formed with an oxidation silicone film with a thickness of 150nm on the above-mentioned ILD film 13. For example, by the plasma-CVD method, this etching stopper layer 14 uses silane system gas like a mono silane (SiH4) or a disilane (Si two H6) for process gas, and is formed. For example, the mono silane (SiH4) and the dinitrogen oxide (N2 O) were used for material gas, and membranes were formed by setting the pressure of 350 degrees C and a membrane formation ambient atmosphere as 1kPa for substrate temperature. The above-mentioned etching stopper layer 14 can also be formed by the silicon acid nitride or the silicon nitride.

[0039] Subsequently, as shown in (2) of drawing 3 , patterning of the above-mentioned etching stopper layer 14 is carried out using a usual lithography technique and a usual etching technique. While forming the opening 15 for forming the connection hole which reaches the 1st above-mentioned wiring 12 to the middle of the above-mentioned etching stopper layer 14, it leaves the above-mentioned etching stopper layer 14 of the bottom of the field which forms slot wiring, and the circumference of it, and other parts remove to the middle of the etching stopper layer 14 to the above-mentioned etching stopper layer 14 by this patterning by etching which used the resist film (not shown) for the etching mask. With the circumference under the field which forms the above-mentioned slot wiring, even if it causes a mask alignment gap in the exposure process at the time of forming a wiring gutter, it considers as the range where a wiring gutter is formed on the etching stopper layer 14.

[0040] The depth which removes the above-mentioned etching stopper layer 14 to the middle is set to 100nm. By this etching, for example using the common plasma etching system, tetrafluoromethane (CF4) and an argon (Ar) were used for etching gas, and the pressure of 1.5kW and an etching ambient atmosphere was set [etching conditions] as 10Pa for RF power as an example. In addition, the etching depth was controlled by etching of the above-mentioned etching stopper layer 14 by controlling etching time. It is necessary to determine that the ILD film 13 will not expose the etching depth at this time all over a wafer in consideration of the homogeneity within a wafer side of an etch rate.

[0041] Then, the usual ashing processing removes the resist film (not shown) used for the above-mentioned etching. In this case, since the ILD film 13 is covered with the etching stopper layer 14, the ILD film 13 is not etched by the above-mentioned ashing processing, and an etching damage does not join the ILD film 13, either.

[0042] Subsequently, by whole surface etchback processing, etchback of the etching stopper layer 14 is carried out, while forming the opening 15 for forming the connection hole which reaches the 1st above-mentioned wiring 12, it leaves the above-mentioned etching stopper layer 14 of the bottom of the field which forms slot wiring, and the circumference of it, and the etching stopper layer 14 of other parts is removed. In addition, let the field which forms the above-mentioned slot wiring, and its circumference be the range which can compensate the mask alignment gap in the lithography technique performed in case patterning for example, of the slot wiring is carried out. In the above-mentioned etchback, using a common plasma etching system, an octafluoro butene (C four F8), an argon (Ar), and a carbon monoxide (CO) are used for etching gas, and etching conditions set the pressure of an etching ambient atmosphere as 6Pa, and set RF power as 1.5kW. As explanation was given [above-mentioned], patterning of the etching stopper layer 14 is carried out by two steps of etching.

[0043] Subsequently, as shown in (3) of drawing 3 , the IMD film 16 which is a wrap thing and turns into an insulator layer during wiring in the above-mentioned etching stopper layer 14 is formed on the above-mentioned ILD film 13. This IMD film 16 is formed with the poly aryl ether by the same formation approach as the above-mentioned ILD film 13. The thickness could be 300nm.

[0044] Furthermore, the hard surface mask blank layer 17 is formed on the above-mentioned IMD film 16. This hard surface mask blank layer 17 deposits and forms silicon oxide in the thickness of 200nm for example, by the plasma-CVD method.

[0045] Subsequently, as shown in (4) of drawing 3 , patterning of the above-mentioned hard surface mask blank layer 17 is carried out using a usual lithography technique and a usual etching technique. First, after forming the resist film

31 on a hard surface mask blank 17, the opening 32 for forming a wiring gutter is formed with a lithography technique.
[0046] Then, as shown in (5) of drawing 3 , the above-mentioned resist film 31 is used for an etching mask, the hard surface mask blank layer 17 is etched, and the opening 18 for forming a wiring gutter is formed. these etching -- as an example -- a magnetron etching system -- using -- etching gas -- an octafluoro butene (C four F8) [supply flow rate -- for example, 10sccm(s) -- setting] and an argon (Ar) -- [-- the supply flow rate used setting] for for example, 200sccm (s) for example, at 2sccm(s), substrate temperature was set as 20 degrees C, and setting] and an oxygen (O2) [supply flow rate set the pressure of 2kW and an etching ambient atmosphere as 8Pa for power.
[0047] Furthermore the hard surface mask blank layer 17 is used for an etching mask, the IMD film 16 is etched, and a wiring gutter 21 is formed. By this etching, the above-mentioned etching stopper layer 14 serves as a pars basilaris ossis occipitalis of a wiring gutter 21, and etching of a wiring gutter 21 is stopped. Then, this etching stopper layer 14 is used for an etching mask, the ILD film 13 is etched from opening 15, and the connection hole 22 which reaches the 1st above-mentioned wiring 12 is formed. By these etching, using a helicon wave plasma etching system as an example, the ammonia (NH3) [supply flow rate used setting] for etching gas for example, at 100sccm(s), and 100 degrees C and source power were set as 1.5kW, and it set [substrate temperature] the pressure of 100W and an etching ambient atmosphere as 1Pa for bias power. Or using a common ECR plasma etching system, nitrogen (N2) and helium (helium) are used for etching gas, and etching conditions set the pressure of an etching ambient atmosphere as 1Pa, and set 1kW and bias RF power as 300W for microwave power.
[0048] In addition, the above-mentioned resist film 31 is removed in case the IMD film 16 and the ILD film 13 are etched. Moreover, when a diffusion prevention layer like a silicon nitride film is formed on the 1st wiring 12, after forming the connection hole 22, anisotropic etching to which the diffusion prevention layer is removed and the front face of the 1st wiring 12 is exposed is performed.
[0049] Moreover, anisotropic etching of the etching stopper layer 14 exposed to the pars basilaris ossis occipitalis of a wiring gutter 21 may be carried out, and it may be removed. This is explained later.
[0050] Then, as shown in (6) of drawing 3 , with sputtering, vacuum deposition, or a CVD method, the barrier metal layer 23 is formed in each inside of the above-mentioned wiring gutter 21 and the connection hole 22, and a copper film is formed further. The barrier metal layer 23 and a copper film are formed also on the hard surface mask blank layer 17 in that case. The above-mentioned barrier metal layer 23 deposits and forms tantalum nitride or a tantalum in the thickness of 50nm. In addition, in order to remove the natural oxidation film currently formed in the front face of the 1st wiring 12 in advance of membrane formation of the barrier metal layer 23, it is desirable to perform sputter etching. And as for after sputter etching, it is desirable to form the barrier metal layer 23, without exposing to an oxidizing quality ambient atmosphere (for example, atmospheric air). For example, the so-called in situ It processes.
[0051] Then, the connection hole 22 and a wiring gutter 21 are embedded with copper with electrolysis plating. A copper film is formed also on the hard surface mask blank layer 17 in that case. Subsequently, while removing the excessive copper film and the barrier metal layer 23 on the hard surface mask blank layer 17 and forming the 2nd wiring 24 in the interior of a wiring gutter 21 by CMP, the plug 25 which connects with the 1st wiring 12 electrically is formed in the interior of the connection hole 22. Although the hard surface mask blank layer 17 serves as a polish stopper in the case of Above CMP, depending on the thickness of the hard surface mask blank layer 17, the hard surface mask blank layer 17 may be removed completely. In addition, in the above-mentioned example, although copper was embedded, you may also embed other metallic materials like aluminum used as a wiring material, for example.
[0052] Although illustration is not carried out, it becomes possible by performing from the formation process of the above-mentioned ILD film 13 to the formation process of wiring 24 and a plug 25 repeatedly further to form a multilayer interconnection.
[0053] Moreover, in the gestalt of implementation of the above 1st, an etching stopper layer may be formed as follows.
[0054] That is, the etching stopper layer 14 is formed the same with said having explained. Then, the above-mentioned etching stopper layer 14 is etched using a usual lithography technique and a usual etching technique. By this etching, using a resist mask, it leaves the above-mentioned etching stopper layer 14 of the bottom of the field which forms slot wiring while forming the opening 15 for forming the connection hole which reaches the 1st above-mentioned wiring 12, and the circumference of it to the above-mentioned etching stopper layer 14, and etching removal of the other parts is carried out. Let the field which forms the above-mentioned slot wiring, and its circumference be the range which can compensate the mask alignment gap in the lithography technique performed in case patterning for example, of the slot

wiring is carried out.
[0055] By etching of the etching stopper layer 14 which consists of the above-mentioned silicon oxide film, for example using the common plasma etching system, tetrafluoromethane (CF4), the argon (Ar), and the carbon monoxide (CO) were used for etching gas as an example, and the pressure of 1.5kW and an etching ambient atmosphere was set [etching conditions] as 6Pa for RF power as an example.
[0056] Subsequently, anisotropic etching removes the above-mentioned resist mask. Anisotropic etching also of the above-mentioned ILD film 13 is carried out in that case. As an example, using a common ECR (Electron Cycrotron Resonance) plasma etching system, nitrogen (N2) and helium (helium) are used for etching gas, and etching conditions set the pressure of an etching ambient atmosphere as 1Pa, and set 1kW and bias RF power as 300W for microwave power by this etching. In addition, since there is an insulator layer 11 in the lower layer of the ILD film 13, this etching stops on an insulator layer 11 at least.
[0057] Then, while embedding the part of the ILD film removed by the above-mentioned etching, the IMD film 16 which is a wrap thing and turns into an insulator layer during wiring in the above-mentioned etching stopper layer 14 is formed on the above-mentioned ILD film 13. This IMD film 16 is formed with the poly aryl ether by the same formation approach as the above-mentioned ILD film 13. The thickness could be 300nm. Subsequent processes are the same with above-mentioned having given explanation.
[0058] SADD of the former [amount / of the etching stopper layer 14 since the opening 15 for forming the connection hole 22 is formed in the etching stopper layer 14 while forming the etching stopper layer 14 only in the perimeter the bottom of the field in which a wiring gutter 21 is formed by the manufacture approach of the semiconductor device explained with the gestalt of implementation of the above 1st] -- it decreases as compared with the etching stopper layer formed of law. usually, the thing for which the amount of the etching stopper layer 14 is reduced in this way although a dielectric constant will become high in order to form an etching stopper layer by the silicon system oxide film, a nitride, etc. -- SADD of the former [dielectric constant / during wiring (between the 2nd wiring 24 and 24), and between wiring layers (between the 1st wiring 12 and the 2nd wiring 24) / effectual] -- it is stopped lower than the thing of a configuration of being formed of law. Therefore, the capacity between wiring and the capacity between wiring are reduced.
[0059] Moreover, since the above-mentioned etching stopper layer 14 is formed only in the perimeter the bottom of the field in which a wiring gutter 21 is formed, when a wiring gutter 21 is formed in the IMD film 16, it will be formed on the etching stopper layer 14, without a wiring gutter 21 protruding the etching stopper layer 14. Therefore, a wiring gutter 21 is formed in the predetermined depth. Moreover, since the etching stopper layer 14 is formed also in the perimeter under the field in which a wiring gutter 21 is formed even if a mask alignment gap occurs in the exposure process of a lithography process in case a wiring gutter 21 is formed, the etching stopper layer 14 is protruded and a wiring gutter 21 is not formed. It seems that therefore, a wiring gutter 21 is formed too much deeply, and the 1st wiring 12 and short circuit are not caused.
[0060] Next, the production process Fig. of drawing 4 explains said explained modification in the gestalt of the 1st operation. The same sign is given to the same thing as the component part shown by said drawing 3 in drawing 4 R> 4.
[0061] As shown in (1) of drawing 4 , a wiring gutter 21 is formed in the condition of penetrating the etching stopper layer 14 and reaching the ILD film 13, in the process shown in (5) of said drawing 3 .
[0062] As shown in (2) of drawing 4 after that, while forming the 2nd wiring 24 in the interior of a wiring gutter 21 through the barrier metal layer 23, a plug 25 is formed in the interior of the connection hole 22 through the barrier metal layer 23 like the process shown in (6) of said drawing 3 R> 3.
[0063] By the manufacture approach shown in above-mentioned drawing 4 , since a wiring gutter 21 is formed also in the etching stopper layer 14, the volume of the part [in which the wiring gutter 21 was formed] of the etching stopper layer 14 has become less than the etching stopper layer 14 of the semiconductor device formed by the manufacture approach shown in drawing 3 . Therefore, the dielectric constant during wiring and between wiring layers only with the effectual part whose volume of the etching stopper layer 14 decreased is reduced.
[0064] In the production process shown in above-mentioned drawing 4 , since a wiring gutter 21 is formed also in the etching stopper layer 14 in case the slot wiring 21 is formed, the volume of the part of the wiring gutter 21 formed in the etching stopper layer 14 becomes less than the etching stopper layer formed by the manufacture approach shown in drawing 3 . Therefore, the effectual dielectric constant during wiring and between wiring layers becomes low.
[0065] Next, the outline configuration sectional view of drawing 5 explains the gestalt of the operation concerning the

2nd semiconductor device of this invention. drawing 5 -- first beer (FV) -- an example of the semiconductor device formed by the approach of this invention based on law is shown.

[0066] As shown in drawing 5 , the wrap insulator layer 51 is formed in a transistor, a capacitor, etc. which are formed on a semi-conductor substrate (not shown) like a silicon substrate (not shown). The wiring 52 of the 1st of slot wiring structure is formed in this insulator layer 51. The ILD (Inter Level Dielectrics) film 53 which serves as an etching stopper layer, covers the 1st above-mentioned wiring 52, and turns into an insulator layer between wiring layers is formed on the bottom of the field which is furthermore on the insulator layer 51, and forms a wiring gutter, and the outskirts of it at the thickness of 300nm. With the circumference under the field which forms the above-mentioned wiring gutter, even if it causes a mask alignment gap in the exposure process at the time of forming a wiring gutter, it considers as the range where a wiring gutter is formed on the etching stopper layer 14. The above-mentioned ILD film 53 is formed with silicon oxide. Or it may be formed with oxidation silicon nitride or silicon nitride.

[0067] Furthermore on the above-mentioned insulator layer 51, the IMD (Inter Metal Dielectrics) film 54 which is a wrap thing and turns into an insulator layer during wiring and between some wiring layers in the above-mentioned ILD film 53 is formed for example, on the ILD film 53 at the thickness of 300nm. This IMD film 54 may be formed by the insulator layer of the same ingredient as the above-mentioned ILD film 53, or may be formed by low dielectric constant organic film, such as BCB film, polyimide film, and amorphous carbon film.

[0068] On the above-mentioned IMD film 54, the hard surface mask blank layer 55 which comes to deposit silicon oxide on the thickness of 200nm is formed. The opening 56 used as a wiring gutter pattern is formed in the hard surface mask blank layer 55. Furthermore a wiring gutter 61 is formed in the ILD film 54 under the above-mentioned opening 56, and the connection hole 62 is formed in the above-mentioned ILD film 54.

[0069] In addition, when a diffusion prevention layer like a silicon nitride film is formed on the 1st wiring 52, the connection hole 62 is formed so that a diffusion prevention layer may be penetrated and the front face of the 1st wiring 52 may be arrived at.

[0070] Furthermore the barrier metal layer 63 is formed in each inside of the above-mentioned wiring gutter 61 and the connection hole 62, the 2nd wiring 64 which consists of copper or a copper alloy is formed in the interior of a wiring gutter 61 through the barrier metal layer 63, and the plug 65 which consists of copper or a copper alloy is formed in the interior of the above-mentioned connection hole 62 through the above-mentioned barrier metal layer 63.

[0071] Furthermore, it is also possible to have formed the ILD film 53 same with above-mentioned having given explanation, the IMD film 54, the connection hole 62, a wiring gutter 61, the 2nd wiring 64, and plug 65 grade on the above-mentioned IMD film 54 and the 2nd wiring 64, and to have carried out the laminating of the above-mentioned wiring structure.

[0072] FV of the former [form / the ILD film 53 of the insulator layer between wiring layers / only in the perimeter / in the 2nd semiconductor device of the above / the bottom of the field in which a wiring gutter 61 is formed] -- the volume has become less than the insulator layer between the wiring layers of the oxidation silicone film formed of law. Usually, when an oxidation silicone film lessens the ILD film 53 which has such a high dielectric constant with about 4.2 dielectric constant since it is high, and is formed, the dielectric constant between wiring (between the 2nd wiring 64 and 64) and between wiring layers (between the 1st wiring 52 and the 2nd wiring 64) is reduced, and the capacity between wiring layers is reduced.

[0073] Next, the production process Fig. of drawing 6 explains the gestalt of the operation concerning the manufacture approach of the 2nd semiconductor device. In drawing 6 , an example of the semiconductor device formed by the approach of this invention based on the FV method is shown, and the same sign is given to the same thing as the component part explained by said drawing 5 .

[0074] Although illustration is not carried out, after forming a transistor, a capacitor, etc. on a semi-conductor substrate (for example, silicon substrate) (not shown), as shown in (1) of drawing 6 , an insulator layer 51 is formed. Subsequently, the 1st wiring 52 is formed in this insulator layer 51 with the slot wiring technique generally known, for example. On the insulator layer 51, for example, by the plasma-CVD method, silicon oxide is deposited on the thickness of 300nm, and the ILD film 53 which is a wrap thing and turns into an insulator layer between wiring layers in the 1st wiring 52 is formed. By this plasma-CVD method, silane system gas like a mono silane (SiH4) or a disilane (Si two H6) is used for process gas. For example, the mono silane (SiH4) and the dinitrogen oxide (N2 O) were used for material gas, and membranes were formed by setting the pressure of 350 degrees C and a membrane formation ambient atmosphere as 1kPa for substrate temperature. In addition, on the ILD film 13, it is also possible to form with

ingredients, such as oxidation silicon nitride and silicon nitride.
[0075] Subsequently, as shown in (2) of drawing 6 , patterning of the above-mentioned ILD film 53 is carried out using a usual lithography technique and a usual etching technique. First, with a lithography technique, after forming the resist film 71 on the ILD film 53, while forming in the above-mentioned resist film 71 the opening 72 for forming the connection hole which reaches the 1st above-mentioned wiring 52, it leaves the above-mentioned resist film 71 on the field which forms a wiring gutter, and its boundary region. Then, by etching which used the resist film 71 for the etching mask, the above-mentioned ILD film 53 is etched, while forming the connection hole 62 which reaches the 1st above-mentioned wiring 52, it leaves the above-mentioned ILD film 53 of the bottom of the field which forms a wiring gutter, and the circumference of it, and the ILD film 53 is removed for other parts. With the circumference under the field which forms the above-mentioned wiring gutter, even if it causes a mask alignment gap in the exposure process at the time of forming a wiring gutter, it considers as the range where a wiring gutter is formed on the ILD film 53. Then, the usual ashing processing removes the above-mentioned resist film 71 used for the etching mask. In addition, the drawing showed the condition before carrying out ashing of the resist film 71.
[0076] Subsequently, as shown in (3) of drawing 6 , on the above-mentioned insulator layer 51, about the above-mentioned ILD film 53, it is a wrap thing, and becomes an insulator layer during wiring, and the insulator layer between some wiring layers forms the IMD film 54. This IMD film 54 is formed with the poly aryl ether by the same formation approach as the above-mentioned ILD film 53. The thickness could be 300nm on the ILD film 53.
[0077] Furthermore, the hard surface mask blank layer 55 is formed on the above-mentioned IMD film 54. This hard surface mask blank layer 55 deposits and forms silicon oxide in the thickness of 200nm for example, by the plasma-CVD method.
[0078] Subsequently, patterning of the above-mentioned hard surface mask blank layer 55 is carried out using a usual lithography technique and a usual etching technique. First, after forming the resist film 73 on a hard surface mask blank 55, the opening 74 for forming a wiring gutter is formed with a lithography technique.
[0079] Then, as shown in (4) of drawing 6 , the above-mentioned resist film 73 is used for an etching mask, the hard surface mask blank layer 55 is etched, and the opening 56 for forming a wiring gutter is formed. these etching -- as an example -- a magnetron etching system -- using -- etching gas -- an octafluoro butene (C four F8) [supply flow rate -- for example, 10sccm(s) -- setting] and an argon (Ar) -- [-- the supply flow rate used setting] for for example, 200sccm (s) for example, at 2sccm(s), substrate temperature was set as 20 degrees C, and setting] and an oxygen (O2) [supply flow rate set the pressure of 2kW and an etching ambient atmosphere as 8Pa for power.
[0080] Furthermore the hard surface mask blank layer 55 is used for an etching mask, the IMD film 54 is etched, and a wiring gutter 61 is formed. By this etching, the above-mentioned ILD film 53 serves as a pars basilaris ossis occipitalis of a wiring gutter 61, and etching which forms a wiring gutter 61 is stopped. Then, opening of the connection hole 62 with which this ILD film 53 was used for the etching mask, and the IMD film 54 was embedded is carried out again. By these etching, using a helicon wave plasma etching system as an example, the ammonia (NH3) [supply flow rate used setting] for etching gas for example, at 100sccm(s), and 100 degrees C and source power were set as 1.5kW, and it set [substrate temperature] the pressure of 100W and an etching ambient atmosphere as 1Pa for bias power. Or using a common ECR plasma etching system, nitrogen (N2) and helium (helium) are used for etching gas, and etching conditions set the pressure of an etching ambient atmosphere as 1Pa, and set 1kW and bias RF power as 300W for microwave power.
[0081] In addition, the above-mentioned resist film 73 is removed in case the IMD film 54 is etched. Moreover, when a diffusion prevention layer like a silicon nitride film is formed on the 1st wiring 52, after forming the connection hole 62, anisotropic etching to which the diffusion prevention layer is removed and the front face of the 1st wiring 52 is exposed is performed.
[0082] Then, as shown in (5) of drawing 3 , with sputtering, vacuum deposition, or a CVD method, the barrier metal layer 63 is formed in each inside of the above-mentioned wiring gutter 61 and the connection hole 62, and a copper film is formed further. The barrier metal layer 63 and a copper film are formed also on the hard surface mask blank layer 55 in that case. The above-mentioned barrier metal layer 63 deposits and forms tantalum nitride or a tantalum in the thickness of 50nm. In addition, in order to remove the natural oxidation film currently formed in the front face of the 1st wiring 52 in advance of membrane formation of the barrier metal layer 63, it is desirable to perform sputter etching. And as for after sputter etching, it is desirable to form the barrier metal layer 63, without exposing to an oxidizing quality ambient atmosphere (for example, atmospheric air). For example, the so-called in situ It processes.

[0083] Then, the connection hole 62 and a wiring gutter 61 are embedded with copper with electrolysis plating. A copper film is formed also on the hard surface mask blank layer 55 in that case. Subsequently, while removing the excessive copper film and the barrier metal layer 63 on the hard surface mask blank layer 55 and forming the 2nd wiring 64 in the interior of a wiring gutter 61 by CMP, the plug 65 which connects with the 1st wiring 52 electrically is formed in the interior of the connection hole 62. Although the hard surface mask blank layer 55 serves as a polish stopper in the case of Above CMP, depending on the thickness of the hard surface mask blank layer 55, the hard surface mask blank layer 55 may be removed completely. In addition, in the above-mentioned example, although copper was embedded, you may also embed other metallic materials like aluminum used as a wiring material, for example.

[0084] Although illustration is not carried out, it becomes possible by performing from the formation process of the above-mentioned ILD film 13 to the formation process of the 2nd wiring 64 and a plug 65 repeatedly further to form a multilayer interconnection.

[0085] By the manufacture approach of the semiconductor device explained with the gestalt of implementation of the above 2nd While forming only in the perimeter the IMD film 54 which is an insulator layer between wiring layers the bottom of the field in which a wiring gutter 61 is formed the former since the connection hole 62 is formed in the ILD film 53 which is an insulator layer during wiring -- FV -- as compared with what was formed of law, the amount of the insulator layer between the wiring layers currently formed with the ingredient which has high dielectric constants, such as a silicon system oxide film, decreases. Thus, by reducing the ILD film 53 which consists of an oxidation silicone film, the dielectric constant between wiring layers (between the 1st wiring 53 and the 2nd wiring 64) is stopped low. Therefore, the capacity between wiring is reduced.

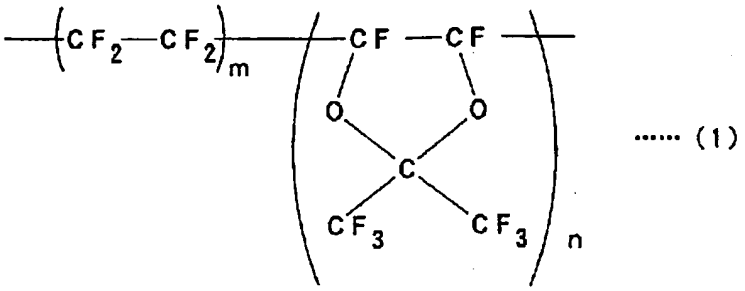
[0086] Moreover, since the ILD film 53 used as an etching stopper layer was formed only in the perimeter the bottom of the field in which a wiring gutter is formed, when a wiring gutter 61 is formed in the IMD film 54 which is an insulator layer during wiring, a wiring gutter 61 separates from the ILD film 53 which is an insulator layer between wiring layers, and is not formed. Therefore, a wiring gutter 61 is formed in the predetermined depth. Moreover, since the layer which has etch selectivity is formed also in the perimeter under the field in which a wiring gutter 61 is formed even if a mask alignment gap occurs in the exposure process of a lithography process in case a wiring gutter 61 is formed, the ILD film 53 is protruded and a wiring gutter 61 is not formed. Therefore, what a wiring gutter 61 is formed too much deeply, and causes the 1st wiring 52 it is [wiring] lower layer wiring, and a short circuit does not happen.

[0087] In addition, the above-mentioned ILD film 13, the IMD film 16, and the above-mentioned IMD film 54 can also be formed with a fluororesin or xerogel. As an example of a fluororesin, fluorocarbon film (for example, [annular fluororesin, Teflon (PTFE), and others]), amorphous Teflon (for example, [Du Pont:Teflon AF (trade name) and others]), and aryl fluoride ether or polyimide fluoride can be used. There is a porous silica as an example of the above-mentioned xerogel.

[0088] In order to form the above-mentioned fluororesin, the precursor of the above-mentioned fluororesin is applied with a rotation coater, and a cure is carried out at 300 degrees C - 450 degrees C after that. In addition, ingredients, such as fluorination amorphous carbon, can form membranes by the plasma-CVD method which used acetylene (C two H2) and fluorocarbon gas [for example, an octafluoro butene (C four F8)] for process gas. After forming membranes also in this case, a cure is carried out at 300 degrees C - 450 degrees C. In addition, if the above-mentioned amorphous Teflon has the structure which it is not limited to Teflon AF and shown in the following chemical formula (1), it is good anything.

[0089]

[Formula 1]



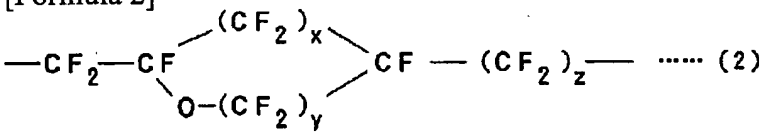
…… (1)

(式中、m、nは正の整数)

[0090] As the above-mentioned ILD film 13 and IMD film 16, it is also possible to use cyclo polymer RAIZUDOFURORINETEDDO polymer system resin [for example, SAITOPPU (trade name)]. If cyclo polymer RAIZUDOFURORINETEDDO polymer system resin has the structure which it is not limited to above-mentioned SAITOPPU and shown in the following chemical formula (2), it is good anything.

[0091]

[Formula 2]



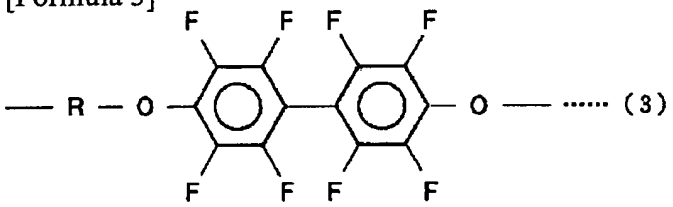
…… (2)

(式中、x、y、zは正の整数)

[0092] As the above-mentioned ILD film 13 and IMD film 16, it is also possible to use fluoride poly allyl compound ether system resin [for example, FLARE (trade name)]. If fluoride poly allyl compound ether system resin has the structure which it is not limited to Above FLARE and shown in the following chemical formula (3), it is good anything.

[0093]

[Formula 3]



…… (3)

(式中、Rはアルキル基)

[0094] Moreover, Nanoporous which the nano glass company developed as an example when the above-mentioned xerogel was used for the above-mentioned ILD film 13 and the IMD film 16 In Silica, membranes were formed using the rotation coater. Above Nanoporous The xerogel which Silica is one sort of a porous silica and can be used by this invention is Above Nanoporous. It is not limited to Silica. Namely, apply on a substrate the silanol resin which has the alkyl group of a macromolecule comparatively, such as aromatic series, and it is made to gel, and if it forms by performing hydrophobing processing using a silane coupling agent or a hydrogen treating, it is applicable no matter it may be what xerogel.

[0095]

[Effect of the Invention] As mentioned above, since opening for forming a connection hole in the etching stopper layer is formed while the etching stopper layer is formed only in the perimeter the bottom of the field in which a wiring gutter is formed according to the 1st semiconductor device of this invention, as explained, the amount of the etching stopper layer formed between two layers of an insulator layer has decreased as compared with the conventional etching stopper layer. Thus, since the amount of the etching stopper layer usually formed with an ingredient with a high

dielectric constant is reduced, the effectual dielectric constant during wiring and between wiring layers is reduced, and reduction of the capacity between wiring and the capacity between wiring layers can be aimed at.

[0096] Since an etching stopper layer is formed only in the perimeter the bottom of the field in which a wiring gutter is formed according to the manufacture approach of the 1st semiconductor device, the amount of the etching stopper layer formed with an ingredient with a high dielectric constant can form few as compared with the conventional etching stopper layer. Therefore, since the effectual dielectric constant during wiring and between wiring layers can be stopped lower than the thing of the conventional configuration, the capacity between wiring and the capacity between wiring can be reduced.

[0097] According to the 2nd semiconductor device, since it is formed only in the perimeter the bottom of the field in which a wiring gutter is formed, the volume of the insulator layer between wiring layers becomes less than the insulator layer between the wiring layers currently formed with the conventional oxidation silicone film. Usually, since an oxidation silicone film is more expensive than about 4.2 dielectric constant and an organic insulating material, by lessening the insulator layer between the wiring layers which have a high dielectric constant and are formed, the effectual dielectric constant between wiring layers is reduced, and it can reduce the capacity between wiring layers.

[0098] Since the insulator layer between wiring layers is formed only in the perimeter the bottom of the field in which a wiring gutter is formed according to the manufacture approach of the 2nd semiconductor device, the amount of the insulator layer during wiring formed with an ingredient with a high dielectric constant can form few as compared with the conventional thing. Therefore, since the effectual dielectric constant of the insulator layer between wiring layers can stop lower than the thing of the conventional configuration, the capacity between wiring layers can be reduced.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is an outline configuration sectional view explaining the gestalt of the operation concerning the 1st semiconductor device of this invention.
[Drawing 2] It is an outline configuration sectional view explaining the modification of the gestalt of the operation concerning the 1st semiconductor device.
[Drawing 3] It is a production process Fig. explaining the gestalt of the operation concerning the manufacture approach of the 1st semiconductor device.
[Drawing 4] It is a production process Fig. explaining the modification of the gestalt of the operation concerning the manufacture approach of the 1st semiconductor device.
[Drawing 5] It is an outline configuration sectional view explaining the gestalt of the operation concerning the 2nd semiconductor device of this invention.
[Drawing 6] It is a production process Fig. explaining the gestalt of the operation concerning the manufacture approach of the 2nd semiconductor device.
[Drawing 7] It is a production process Fig. explaining the conventional SACC method.
[Description of Notations]
13 [-- The IMD film, 21 / -- A wiring gutter, 22 / -- Connection hole] -- The ILD film, 14 -- An etching stopper layer, 15 -- Opening, 16

[Translation done.]